CURRICULUM VITAE

CV date	03/09/2020

Part A. PERSONAL INFORMATION

First and Family name	Alfonso Sánchez-Macián Pérez	
Researcher codes	WoS Researcher ID	K-1619-2014
	SCOPUS Author ID	23398740500
	Open Researcher and Contributor ID (ORCID)	0000-0002-2220-0594

A.1. Current position

Name of University/Institution	Universidad Antonio de Nebrija			
Department	ARIES Research Center			
Address and Country	C/ Pirineos 55, Madrid			
Phone number	914521100	E-mail	asanchep@nebrija.es	
Current position	Associate Professor		From	10/07/2010
Key words	Reliability, Fault tolerance			

A.2. Education

PhD	University	Year
PhD on Telecommunication Engineering	Universidad Politécnica de Madrid	2007

A.3. JCR articles, h Index, thesis supervised…

***Information from Web of Science*:**

Sum of times cited: 238
Average citations per year, last five years: 31 Detail for 2015-2019 [33, 25, 30, 25, 42]
h-Index (Scopus): 8 h-Index (Google Scholar): 10

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

Alfonso Sánchez-Macián received the M.Sc. and Ph.D. degrees in telecommunications engineering from Universidad Politécnica de Madrid in 2000 and 2007, respectively. He has worked as a Lecturer and a Researcher at several universities, such as the Universidad Politécnica de Madrid; IT Innovation Centre, University of Southampton, Southampton, U.K.; and the Universidad Antonio de Nebrija, Madrid. At Universidad Antonio de Nebrija, he was appointed as CIO (2010-2014), Vice Rector for Education and Academic Affairs (2013-2015) and Director of the Computer Engineering Program (2016-2018). He previously worked in numerous national and multinational companies as a Project Manager and a Senior Consultant for IT projects.

In terms of research, he has published 26 papers in JCR-indexed journals, a book chapter (Wiley) and several publications in congresses and workshops. He has taken part in 8 research projects and 1 R+D contract. He was awarded by the Official College of Telecommunication Engineers with the Prize to the best Thesis in the topic of Management and regulation of Telecommunications. He is currently part of the ARIES (Aerospace Research and Innovation in Electronic Systems) Research Center, where he focuses on fault tolerance in electronic systems and processor in the Space environment.

Regarding teaching duties, he has taught more than 1200 hours of lectures at the university at bachelor and master levels, in Computer Engineering, Industrial Engineering, Telecommunication Engineering, Business Administration, Tourism and Marketing degrees. He is currently Director for the Industrial Technology PhD program.

Part C. RELEVANT MERITS

C.1. Publications (including books) [2017-2020]

[1] F. Garcia-Herrero, A. Sanchez-Macian and J. A. Maestro, "Combined symbol error correction and spare through-silicon vias for 3D memories," in IEEE Transactions on Emerging Topics in Computing (on press).

[2] K.W. Gear, A. Sánchez-Macián, F. Garcia-Herrero, J.A. Maestro, “Two Behavioural Error Detection Techniques for the Cascaded Integrator–Comb Interpolation Filter Implemented on FPGA”. Circuits, Systems and Signal Processing (2020).

[3] F. Garcia-Herrero, A. Sánchez-Macián, M. San-Isidro, L. A. Aranda and J. A. Maestro, "Efficient Majority-Logic Reed-Solomon Decoders for Single Symbol Correction," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 2, pp. 390-394, June 2020

[4] L.A. Aranda, N-J Wessman, L. Santos, A. Sánchez-Macián, J. Andersson, R. Weigand, J.A. Maestro, “Analysis of the Critical Bits of a RISC-V Processor Implemented in an SRAM-Based FPGA for Space Applications”. Electronics 2020, 9, 175

[5] L. A. Aranda, A. Sánchez-Macián and J. A. Maestro, "An Algorithmic-Based Fault Detection Technique for the 1-D Discrete Cosine Transform," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 5, pp. 1336-1340, May 2020

[6] L. A. Aranda, F. Garcia-Herrero, L. Esteban, A. Sánchez-Macián and J. A. Maestro, "Radiation Hardened Digital Direct Synthesizer With CORDIC for Spaceborne Applications," in IEEE Access, vol. 8, pp. 83167-83176, 2020.

[7] A. Sánchez-Macián, L.A. Aranda, P. Reviriego, J.A. Maestro, “Reducing false positives due to double adjacent errors in instruction TLBs”, Microelectronics Reliability, Volume 102, November 2019,

[8] A. Das, A. Sánchez-Macián, F. García-Herrero, N. A. Touba and J. A. Maestro, "Enhanced Limited Magnitude Error Correcting Codes for Multilevel Cell Main Memories," in IEEE Transactions on Nanotechnology, vol. 18, pp. 1023-1026, 2019.

[9] L. A. Aranda, A. Sánchez-Macián and J. A. Maestro, "ACME: A Tool to Improve Configuration Memory Fault Injection in SRAM-Based FPGAs," in IEEE Access, vol. 7, pp. 128153-128161, 2019.

[10] A. Sánchez-Macián, F. Garcia-Herrero, J.A. Maestro, “Reliability of 3D memories using Orthogonal Latin Square codes”, Microelectronics Reliability (ISSN 0026-2714), Vol. 95, April 2019, Pages 74-80

[11] A. Sánchez-Macián, L. A. Aranda, P. Reviriego, V. Kiani and J. A. Maestro, "Enhancing Instruction TLB Resilience to Soft Errors," in IEEE Transactions on Computers, vol. 68, no. 2, pp. 214-224, 1 Feb. 2019.

[12] A. Ullah, P. Reviriego, A. Sánchez-Macián and J. A. Maestro, "Multiple Cell Upset Injection in BRAMs for Xilinx FPGAs," in IEEE Transactions on Device and Materials Reliability, vol. 18, no. 4, pp. 636-638, December 2018.

[13] J. Tabero, A. Regadío, C. Pérez, J. Pazos, P. Reviriego, A. Sánchez-Macián, J.A. Maestro, “Modular fault tolerant processor architecture on a SoC for space”, Microelectronics Reliability, Elsevier (ISSN: 0026-2714), Vol. 83, April 2018, pp. 84-90.

[14] A. Sánchez-Macián, P. Reviriego, J. Tabero, A. Regadío, J.A. Maestro, “SEFI Protection for Nanosat 16-Bit Chip Onboard Computer Memories”, IEEE Transactions on Device and Materials Reliability (ISSN: 1530-4388), Vol 17, no 4, December 2017, pp. 698-707.

[15] A. Sánchez-Macián, P. Reviriego, J.A. Maestro, S. Liu, "Single Event Transient Tolerant Bloom Filter Implementations", IEEE Transactions on Computers (ISSN: 0018- 9340), Vol 66, No 10, October 2017, pp. 1831-1836.

[16] P. Reviriego, S. Liu, A. Sánchez-Macián, L. Xiao, J.A. Maestro, "A Scheme to Reduce the Number of Parity Check Bits in Orthogonal Latin Square Codes", IEEE Transactions on Reliability (ISSN: 0018-9529), Vol. 66, No 2, June 2017, pp. 518-528.

[17] A. Sánchez-Macián, P. Reviriego, J.A. Maestro, "Combined Modular Key and Data Error Protection for Content-Addressable Memories", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 66, No 6, June 2017, pp. 1085-1090.

C.2. Research projects and grants

1) Project Title: Introduction of fault-tolerant concepts for RISC-V in space applications
   Funding entity: European Space Agency - Innovation Triangle Initiative (ITI).
   Partners: Gaisler (coordinador), Universidad Antonio de Nebrija, QinetiQ.
   2018- 2019 Allocated budget: 67.000
   Principal investigator: Jan Andersson (Gaisler). Juan Antonio Maestro (Nebrija)
   Role: Researcher.

2) Project Title: Design, implementation and experimentation of fault tolerance techniques for multi-processor systems in on-board Space applications (ESP2014-54505-C2-1-R)
   Funding entity: Ministerio de Economía y Competitividad
   Partners: Universidad Antonio de Nebrija, Instituto Nacional de Técnica Aeroespacial
   2015- 2017 Allocated budget: 127.050
   Principal investigator: Juan Antonio Maestro
   Role: Researcher.

3) Project Title: Space Ethernet Physical Layer Transceiver (SEPHY)
   Funding entity: UNIÓN EUROPEA (HORIZON 2020)
   Partners: ARQUIMEA INGENIERIA S.L, THALES ALENIA SPACE ESPANA SA, UNIVERSITAS NEBRISSENSIS SA, IHP GMBH, ATMEL NANTES SAS, TTTECH COMPUTERTECHNIK AG
   01/05/2015- 01/08/2018 Allocated budget: 359.350
   Principal investigator: Pedro Reviriego
   Role: Researcher.

C.3. Contracts

- Project Title:New Protocol Semantics and Scheduling Primitives for Energy
  Contract modality: Research Award
  Funding entity: Google Inc.
  Partners:Universidad Antonio de Nebrija y University of South Florida
  01/12/2011-01/12/2012 Allocated budget: 10.000 USD
  Principal investigator: Pedro Reviriego y Ken Christensen
  Role: Researcher.

C.4. Patents

C.5. Awards

COIT Award to the best Thesis in the topic of Management and regulation of Telecommunications.

C.6. International mobility

- Centre: IT Innovation Centre (University of Southampton)
  City: Southampton
  Country: Reino Unido
  Starting Date: 01/01/2007
  Duration (weeks): 61
  Topic: GRIA (Commercial GRID tool) R+D team.
  Permanent contract.