CURRICULUM VITAE

Part A. PERSONAL INFORMATION

CV date	27-09-2019

First and Family name	Juan Antonio Maestro de la Cuerda	
Researcher codes	WoS Researcher ID *(*)*	L-6091-2014
	SCOPUS Author ID*(*)*	8664715000
	Open Researcher and Contributor ID (ORCID) **	0000-0001-7133-9026

A.1. Current position

Name of University/Institution	Universidad Antonio de Nebrija			
Department	ARIES Research Center			
Address and Country	Pirineos, 55 – 28040 Madrid			
Phone number	914521100	E-mail	jmaestro@nebrija.es	
Current position	Professor		From	01/09/2004
UNESCO codes	3304, 3307			
Key words	Electronics, Reliability, Computer Systems, Processors			

A.2. Education

Diploma	University	Year
Ph.D. (Computer Architecture)	Universidad Complutense de Madrid	1999
M.Sc. (Physics)	Universidad Complutense de Madrid	1994

A.3. JCR articles, h Index, thesis supervised…

Number of publications: 173.
Number of Q1: 30
h-index: 20 (Scopus).
Total citations: 1634 (Scopus).
Average citations/year in the last 5 years: 206 (Scopus).
Supervised thesis (2011-2019): 7.

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

Juan Antonio Maestro received the M.Sc. degree in physics and the Ph.D. degree in computer engineering from Universidad Complutense de Madrid, Madrid, Spain, in 1994 and 1999, respectively. He has directed, since 2004, the Electronic Design and Space Technology research group at Universidad Nebrija, Madrid, Spain, where he has also recently founded the ARIES research center (www.nebrija.es/aries), devoted to the Aerospace Research and Innovation in Electronic Systems. His current activities are oriented to the space industry, with several projects on the protection of digital circuits against the effects of radiation, including microprocessors, memories and auxiliary systems. He also collaborates with institutions as the European Space Agency, Stanford University, University College Dublin or the Harbin Institute of Technology, among others. He is the author of more than 150 publications, both in journals and international conferences, as well as some patents in the field of fault-tolerant digital circuits. His areas of interest include computer architecture, digital design, fault-tolerance, reliability, small satellites and space applications.

Part C. RELEVANT MERITS

C.1. Publications (including books)

1. A. Ramos, R. González-Toral, P. Reviriego, J.A. Maestro, "An ALU protection methodology for soft processors on SRAM-based FPGAs", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 68, No 9, September 2019, pp. 1404–1410.

2. A. Ullah, P. Reviriego, J.A. Maestro, "An efficient methodology for on-chip SEU injection in flip-flops for Xilinx FPGAs", IEEE Transactions on Nuclear Science (ISSN: 0018-9499), Vol. 65, No 4, April 2018, pp. 989-996.

3. P. Reviriego, S. Liu, A. Sánchez-Macián, L. Xiao, J.A. Maestro, "A Scheme to Reduce the Number of Parity Check Bits in Orthogonal Latin Square Codes", IEEE Transactions on Reliability (ISSN: 0018-9529), Vol. 66, No 2, June 2017, pp. 518-528.

4. A. Sánchez-Macián, P. Reviriego, J.A. Maestro, "Combined Modular Key and Data Error Protection for Content-Addressable Memories", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 66, No 6, June 2017, pp. 1085-1090.

5. M. Demirci, P. Reviriego, J.A. Maestro, "Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 65, No 9, September 2016, pp. 2932-2938.

6. P. Reviriego, S. Pontarelli, A. Evans, J.A. Maestro, "A Class of SEC-DED-DAEC codes derived from Orthogonal Latin Square Codes", IEEE Transactions on Very Large Scale Integration (VLSI) Systems (ISSN: 1063-8210), Vol. 23, No 5, May 2015, pp. 968-972.

7. C. Argyrides, P. Reviriego, J.A. Maestro, "Using Single Error Correction Codes to Protect Against Isolated Defects and Soft Errors", IEEE Transactions on Reliability (ISSN: 0018-9529), Vol. 62, No 1, March 2013, pp. 238-243.
8. P. Reviriego, C. Bleakley, J.A. Maestro, "Diverse Double Modular Redundancy: A New Direction for Soft Error Detection and Correction", IEEE Design & Test of Computers (ISSN: 0740-7475), Vol. 30, No 2, March-April 2013, pp. 87-95.
9. P. Reviriego, S. Pontarelli, J.A. Maestro, M. Ottavi, "A Method to Construct Low Delay Single Error Correction (SEC) Codes for Protecting Data Bits Only", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (ISSN: 0278-0070), Vol. 32, No 3, March 2013, pp. 479-483.
10. P. Reviriego, M. Flanagan, S. Liu, J.A. Maestro, "Multiple Cell Upset Correction in Memories Using Difference Set Codes", IEEE Transactions on Circuits and Systems I (ISSN: 1549-8328), Vol. 59, No 11, November 2012, pp. 2592-2599.

C.2. Research projects and grants

1. Project title: "Introduction of fault-tolerant concepts for RISC-V in space applications"
   Funding entity: European Space Agency (ESA)
   Participants: Universidad Antonio de Nebrija, Cobham Gaisler AB and QinetiQ Space NV.
   Duration, from: 05/2018 to: 10/2019
   Amount: 67.334 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

2. Project title: " Diseño, implementación y experimentación de técnicas de tolerancia a fallos para sistemas multi-procesador en aplicaciones espaciales embarcadas" (ESP2014-54505-C2-1-R).
   Funding entity: Ministerio de Economía y Competitividad – Plan Nacional de Espacio.
   Participants: Universidad Antonio de Nebrija, INTA.

Duration, from: 01/2015 to: 12/2017
Amount: 127.050 EUR
Principal investigator: Juan Antonio Maestro de la Cuerda.

3. Project title: “Space Ethernet Physical Layer Transceiver (SEPHY)" (Proposal 640243 [COMPET-01-2014]).
   Funding entity: Comisión Europea – Horizonte 2020.
   Participants: Arquímea (coordinador), Universidad Antonio de Nebrija, Thales Alenia, Atmel, IHP y TTTech.
   Duration, from: 05/2015 to: 12/2018
   Amount: 359.350 EUR
   Principal investigator: Daniel González Gutiérrez (Arquímea)

4. Project title: “Diseño, simulación y experimentación con radiación sobre memorias y otros circuitos digitales complejos para aplicaciones espaciales embarcadas" (AYA2009-13300-C03-01).
   Funding entity: Ministerio de Ciencia e Innovación. – Plan Nacional de Espacio
   Participants: Universidad Antonio de Nebrija, Universidad Complutense de Madrid.
   Duration, from: 01/2010 to: 12/2012
   Amount: 118.000 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

5. Project title: "RadEsSim - Estudio de la Radiación en el Espacio: Simulación de los Efectos en Circuitos Digitales y Diseño de Implementaciones Tolerantes a Fallos" (1/2007).
   Funding entity: Comunidad de Madrid – Plan Aeroespacial.
   Participants: Universidad Antonio de Nebrija.
   Duration, from: 01/2007 to: 12/2008
   Amount: 75,887 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

C.3. Contracts

1. Contract title: "New Protocol Semantics and Scheduling Primitives for Energy Efficiency: Burst Coalescing at the Link and Application Layers"
   Type: Google Research Award
   Funding entity: Google Inc
   Participants: Universidad Antonio de Nebrija/Universidad de South Florida
   Duration, from: 15/12/2011 to: 15/12/2012
   Principal researcher: Pedro Reviriego Vasallo/Ken Christensen

2. Contract title: "ExhaustiF®-MFA: Modelo de Fallos Avanzados para la plataforma ExhaustiF®", (A/000613/09)
   Type: Subcontratación
   Funding entity: Métodos y Tecnología de Sistemas y Procesos, S.L.
   Participants: Universidad Antonio de Nebrija
   Duration, from: 01/01/2009 to: 30/06/2010
   Principal researcher: Pedro Reviriego Vasallo

3. Contract title: "Estudio del consumo energético en el uso de las TIC" (PK09-005555-TE)
   Type: Subcontratación
   Funding entity: Telefónica de España
   Entities: Universidad Antonio de Nebrija
   Participants, from: 01/11/2008 to: 01/06/2009
   Principal researcher: Pedro Reviriego Vasallo

4. Contract title: "Energy Efficient Communications: Improving Energy Consumption in Ethernet"
   Type: Google Research Award

Funding entity: Google Inc
Participants: Universidad Complutense de Madrid, Universidad Antonio de Nebrija
Duration, from: 01/09/2009 to: 01/09/2010
Principal researcher: Pedro Reviriego Vasallo

C.4. Patents

1. Inventors: Juan Antonio Maestro, Pilar Reyes, Oscar Ruano, Pedro Reviriego
   Title: "Método de detección y corrección de errores producidos por los efectos de la radiación en filtros de media móvil"
   Application no.: P200602433 Country: Spain
   Date: 11-10-2010
   Entity: Universidad Antonio de Nebrija, Universidad Carlos III de Madrid
2. Inventors: Juan Antonio Maestro, Pilar Reyes, Oscar Ruano, Pedro Reviriego
   Title: "Filtro de media móvil y método para la detección y corrección de errores utilizando paridad bidimensional"
   Application no.: P200930207 Country: Spain
   Date: 26-01-2011
   Entity: Universidad Antonio de Nebrija, Universidad Carlos III de Madrid
3. Inventors: Juan Antonio Maestro, Pilar Reyes, Oscar Ruano, Pedro Reviriego
   Title: "Método y filtro de media móvil para la detección y corrección de errores por medio de un filtro diezmado"
   Application no.: P200930205 Country: Spain
   Date: 16-05-2011
   Entity: Universidad Antonio de Nebrija, Universidad Carlos III de Madrid

C.5. Research Visits

University: Stanford University
City, Country: Stanford, USA
Date: July – September 2013
Duration (weeks): 10
Topic: Study of the reliability of complex multi-processor systems.

C.6. Awards

- *Premio Extraordinario de Licenciatura*, Universidad Complutense de Madrid, year 1994.
- *Premio Extraordinario de Doctorado*, Universidad Complutense de Madrid, year 1999.

C.7. Misc.

- *Catedrático de Universidad* accreditation, ANECA (January 2013).
- *Profesor Titular de Universidad* accreditation, ANECA (March 2009).
- Director of the ARIES Research Center (2016 -).
- Vice-rector for Research, Universidad Antonio de Nebrija (July 2010 - August 2014).
- Chair of the Computer Engineering Department (2009-2010 and 2016 -)
- ANEP expert (2009 –).
- European Commission expert (Horizon 2020).
- IEEE Senior Member (2015 -) , IEEE Member (2007-2014)
- Reviewer for serveral technical journals (IEEE Transactions on Nuclear Science, IEEE Transactions on Device and Materials Reliability, …).