CURRICULUM VITAE

CV date	16/09/2019

Part A. PERSONAL INFORMATION

First and Family name	Luis Alberto Aranda Barjola	
Researcher codes	WoS Researcher ID *(*)*	F-1400-2015
	SCOPUS Author ID*(*)*	
	Open Researcher and Contributor ID (ORCID) **	0000-0003-4458-9761

(*) At least one of these is mandatory
(**) Mandatory

A.1. Current position

Name of University/Institution	Universidad Antonio de Nebrija			
Department	ARIES Research Center			
Address and Country	C/ Pirineos 55, 28040			
Phone number	914521100	E-mail	laranda@nebrija.es	
Current position	Assistant Professor		From	01/02/2018
Key words	Electronics, Reliability, FPGA, Microprocessor, Fault tolerance			

A.2. Education

PhD	University	Year
PhD in Industrial Engineering	Universidad Antonio de Nebrija	2018
MSc in Robotics	Universidad Carlos III de Madrid	2015
BSc in Industrial Engineering	Universidad Carlos III de Madrid	2012

A.3. JCR articles, h Index, thesis supervised…

The following indicators have been obtained from Google Scholar database:
· Total number of cites (from 2014): 21
· Number of Q1 publications: 3
· h index: 2

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

I received a B.Sc. in Industrial Engineering (2012) and a M.Sc. in Robotics (2015) from Universidad Carlos III de Madrid, and a Ph.D. in Industrial Engineering (2018) from Universidad Antonio de Nebrija. I have worked as a Project Engineer at Zeus Creative Technologies S.L. developing various Computer Vision projects from 2013 to 2014. I was responsible for both hardware and software design and implementation. Currently I am an assistant professor at Universidad Antonio de Nebrija and part of the ARIES Research Center, in which I develop my research lines.

My research lines are related to digital electronics reliability. In my thesis, I proposed several ad-hoc techniques to protect a star tracker system against the effects of space radiation. In order to do that, I built from scratch this optical system used to determine the attitude of the satellites. Within the framework of my thesis, I also did a three-months stay in the European Space Agency (ESA) at Noordwijk (The Netherlands).

To date, I have written 13 scientific papers. Seven of them have been published in journals indexed in JCR, and two of them in international congresses. The remaining four papers are currently under review in JCR-indexed journals.

Part C. RELEVANT MERITS

C.1. Publications (including books)

1. A. Sánchez-Macián, L.A. Aranda, P. Reviriego, J.A. Maestro, “Reducing False Positives due to Double Adjacent Errors in Instruction TLBs”, Microelectronics Reliability (ISSN: 0026-2714), Vol. 102, November 2019, p. 113494.
2. L.A. Aranda, A. Sánchez-Macián, J.A. Maestro, “COMET: A Tool to Improve Configuration Memory Fault Injection in SRAM-based FPGAs”, IEEE Access (ISSN: 2169-3536), Vol. 4, September 2019.
3. A. Sánchez-Macián, L.A. Aranda, P. Reviriego, V. Kiani, J.A. Maestro, “Enhancing Instruction TLB Resilience to Soft Errors”, IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 68, No 2, February 2019, pp. 214-224.
4. L.A. Aranda, P. Reviriego, R. González-Toral, J.A. Maestro, "Protection Scheme for Star Tracker Images", IEEE Transactions on Aerospace and Electronic Systems (ISSN: 0018-9251), Vol. 55, No 1, February 2019, pp. 486-492.
5. L.A. Aranda, P. Reviriego, J.A. Maestro, “Protecting Image Processing Pipelines against Configuration Memory Errors in SRAM-based FPGAs”, MDPI Electronics (ISSN: 2079-9292), Vol. 7, No 11, November 2018, p. 322.
6. L.A. Aranda, P. Reviriego, J.A. Maestro, "A Comparison of Dual Modular Redundancy and Concurrent Error Detection in Finite Impulse Response (FIR) Filters Implemented in SRAM-based FPGAs through Fault Injection", IEEE Transactions on Circuits and Systems II (ISSN: 1549-7747), Vol. 65, No 3, March 2018, pp. 376-380.
7. L.A. Aranda, P. Reviriego, J.A. Maestro, "Error Detection Technique for a Median Filter", IEEE Transactions on Nuclear Science (ISSN: 0018-9499), Vol. 64, No 8, August 2017, pp. 2219-2226.
8. L.A. Aranda, P. Reviriego, J.A. Maestro, "Design Placement Guidelines for Single Event Upset (SEU) Minimization in SRAM-based FPGAs", Design of Circuits and Integrated Systems Conference (DCIS2017), Barcelona (Spain), November 22-24, 2017.
9. L.A. Aranda, P. Reviriego, J.A. Maestro, "A Fault-Tolerant Implementation of the Median Filter", Proc. of the RADECS 2016 conference, Bremen (Germany), September 19-23, 2016.

C.2. Research projects and grants

1. Project title: "Introduction of fault-tolerant concepts for RISC-V in space applications"
   Funding entity: European Space Agency (ESA)
   Participants: Universidad Antonio de Nebrija, Cobham Gaisler AB and QinetiQ Space NV.
   Duration: From May-2018 to Oct-2019
   Amount: 67.334 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

2. Project title: "Diseño, implementación y experimentación de técnicas de tolerancia a fallos para sistemas multi-procesador en aplicaciones espaciales embarcadas" (ESP2014-54505-C2-1-R).
   Funding entity: Ministerio de Economía y Competitividad – Plan Nacional de Espacio.
   Participants: Universidad Antonio de Nebrija, INTA.
   Duration: From Jan-2015 to Dec-2017
   Quantity of the grant: 127.050 EUR
   Principal researcher: Juan Antonio Maestro de la Cuerda.

C.3. Contracts

C.4. Patents

C.5, C.6, C.7… (e. g., Institutional responsibilities, memberships of scientific societies…)

Awards:

- (2018) International Mention of the PhD Thesis
- (2019) Extraordinary doctorate award