CURRICULUM VITAE

Part A. PERSONAL INFORMATION

CV date	16/09/2019

First and Family name	Francisco Miguel García Herrero	
Researcher codes	WoS Researcher ID *(*)*	
	SCOPUS Author ID*(*)*	53877344900
	Open Researcher and Contributor ID (ORCID) **	0000-0001-6719-9681

(*) At least one of these is mandatory
(**) Mandatory

A.1. Current position

Name of University/Institution	Universidad Antonio de Nebrija			
Department	ARIES Research Center			
Address and Country	Spain			
Phone number	+34914521100	E-mail	fgarciahe@nebrija.es	
Current position	Associate Professor		From	03/09/18
Key words	Computer and electronics engineering,			

A.2. Education

PhD	University	Year
Electronics engineering	Universitat Politècnica de València	2013

A.3. JCR articles, h Index, thesis supervised

- JCR articles: 18, (2-Q3, 14-Q2, 2-Q1)
- h-Index: 8
- Average number of citations: 6.18
- Total number of citations: 167
- Thesis supervised: 2
  - https://riunet.upv.es/handle/10251/73266
  - https://riunet.upv.es/handle/10251/86152

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

Since 2011, the main research line is the design and implementation of algorithms and hardware architectures for Forward Error Correction (FEC) codes required in modern communication and storage systems, such as flash memories, satellite decoders and long-haul optical fiber-optic networks. The research is focused on:

- Low density binary decoders, LDPC
- Low-density non-binary parity code decoders, NB-LDPC
- Polar codes decoders
- Soft decoding of the Reed-Solomon codes

The objective is to improve the performance of the decoders trying to balance coding gain, throughput, latency and area resources, by means of reducing complexity in decoding algorithms with a negligible loss in error correction. In addition, solutions to mitigate the error floor effect of low complexity algorithms based on majority logic decoding have been studied through real implementations in field-programmable gate array (FPGA) of several decoder architectures.

Related to these topics, more than fifteen articles have been published in journals included in the Journal Citation Reports (JCR) in the field of Electrical and Telecommunications Engineering (Q1-Q2). In addition, a patent for the architecture of a new decoding algorithm for non-binary LDPC codes, which can be applied to fault-tolerant flash memories and other modern storage devices, was registered. All this production is supported by competitive projects of the Spanish Government (3 projects since 2009) and drove international collaborations with the Equipes Traitement de l'Information et Systèmes (Ecole Nationale Supérieure de l'Electronique et de ses Applications), the Department of Electrical and Computer Engineering (University of California) and School of Electrical and Electronic Engineering (University College Dublin).

Medium and long term research will continue with error correction decoders and fault tolerance processing architectures for high-performance systems in order to provide new algorithms and designs to satisfy the requirements of demanding areas such as space technology.

Part C. RELEVANT MERITS

C.1. Publications (including books)

JCR articles

1. J. Valls, V. Torres, M. J. Canet and **F. M. Garcia-Herrero**, "A Test Vector Generation Method Based on Symbol Error Probabilities for Low-Complexity Chase Soft-Decision Reed–Solomon Decoding," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 6, pp. 2198-2207, June 2019. **Q1**
2. Jesús Omar Lacruz Lucht; **Francisco Miguel García Herrero**; MJ Canet Subiela; Javier Valls Coquillat. High-performance NB-LDPC decoder with reduction of message exchange. IEEE Transactions on Very Large Scale Integration. Vol. 24, No. 5, pp. 1950-1961, May 2016. **Q2**
3. Jesús Omar Lacruz Lucht; **Francisco Miguel García Herrero**; MJ Canet Subiela; Javier Valls Coquillat. Reduced-complexity Non-Binary LDPC decoder for high-order Galois fields based on Trellis Min-Max algorithm. IEEE Transactions on Very Large Scale Integration. Vol. 24, No. 8, pp. 2643-2653, August 2016. **Q2**
4. Jesús Omar Lacruz Lucht; **Francisco Miguel García Herrero**; David Declercq; Javier Valls Coquillat. One Minimum Only Trellis Decoder for Non-Binary Low-Density Parity-Check Codes. IEEE Transactions on Circuits and Systems I. Vol.62, No.1, pp.177-184, January 2015. **Q1**
5. Jesús Omar Lacruz Lucht; **Francisco Miguel García Herrero**; Javier Valls Coquillat. Reduction of complexity for Nonbinary LDPC decoders with compressed messages. IEEE Transactions on Very Large Scale Integration. Vol. 23, no. 11, pp. 2676-2679, November. 2015. **Q2**
6. Jesus Omar Lacruz Lucht; **Francisco Miguel García Herrero**; David Declercq; Javier Valls Coquillat. Simplified Trellis Min- Max Decoder Architecture for Nonbinary Low-Density Parity-Check Codes. IEEE Transactions on Very Large Scale Integration. Vol. 23, No. 9, pp.1783-1792, September 2015. **Q2**
7. **Francisco Miguel García Herrero**; Erbao Li; David Declercq; Javier Valls Coquillat. Multiple-Vote Symbol Flipping Decoder for Non-Binary LDPC Codes. IEEE Transactions on Very Large Scale Integration. Vol.22, No.11, pp.2256-2267, November 2014. **Q2**
8. **Francisco Miguel García Herrero**; MJosé Canet Subiela; Javier Valls Coquillat. Non-Binary LDPC Decoder Based on Simplified Enhanced Generalized Bit Flipping Algorithm. IEEE Transactions on Very Large Scale Integration. Vol.22, No.6, pp.1455-1459, June 2014. **Q2**
9. **Francisco Miguel García Herrero**; MJosé Canet Subiela; Javier Valls Coquillat. Non-Binary LDPC Decoder Based on Symbol Flipping with Multiple Votes. IEEE Communications Letters. Vol.18, No.5, pp.749-752, June 2014. **Q2**
10. **Francisco Miguel García Herrero**; MJosé Canet Subiela; Javier Valls Coquillat. Architecture of Generalized Bit-Flipping Decoding for High-Rate Non-binary LDPC Codes. Circuits, Systems, and Signal Processing. Vol.32 No.2, pp.727-741, April 2013. **Q2**

C.2. Research projects and grants

1. **Project Reference:** TEC2015-70858-C2-2-R
   Title: Tratamiento Digital de la Señal y Corrección de Errores en Transmisión Óptica Mediante Fibra Multi-Núcleo Para Redes Ópticas De Acceso Y De Transporte Celular
   Principal investigator: Javier Valls Coquillat y Vicenç Almenar Terre
   Funding entity: Ministerio de Economía y Competitividad. Gobierno de España.
   Duration: 01/01/2016 - 31/12/2018
   Allocated Budget: 190.817 €
   Project status: Approved
2. **Project Reference:** TEC2011-27916
   Title: Algoritmos y arquitecturas de FEC para futuros sistemas de comunicaciones
   Principal investigator: Javier Valls Coquillat
   Funding entity: Ministerio de Ciencia e Innovación. Gobierno de España.
   Duration: 01/01/2012 - 31/12/2014
   Allocated Budget: 147.862 €
   Project status: Approved
3. **Project Reference:** TEC2008-06787
   Title: Arquitecturas de FEC para sistemas de comunicaciones de muy alta velocidad
   Principal investigator: Javier Valls Coquillat
   Funding entity: Ministerio de Ciencia e Innovación. Gobierno de España.
   Duration: 01/01/2009- 31/12/2011
   Allocated Budget: 129.833 €
   Project status: Approved
4. **Project Reference:** PAID-06-07-002-303
   Title: Generación-detección en banda base de señales QAM ultra anchas
   Principal investigator: MªAsunción Pérez Pascual
   Funding entity: Universitat Politècnica de València.
   Duration: 04/12/07- 04/12/09
   Allocated Budget: 10.600€
   Project status: Approved
5. **Grant Reference:** AP2010-5178
   Title: Formación del Profesorado Universitario (FPU-Grant/Contract)
   Funding entity: Ministerio de Educación, Cultura y Deporte.
   Duration: 04/12/07- 04/12/09
   Allocated Budget: 35.614,56€

C.3. Contracts

C.4. Patents

- **European Patent:** Method for decoding non-binary codes and corresponding decoding apparatus
  Number of patent: 14 290 024.0
  Inventors: Francisco Miguel García Herrero, Javier Valls, David Declerq, Erbao Li
  Ownership: Universidad Politécnica de Valencia y University Cergy-Pontoise
  Date: 03/02/2014

C.5. Awards

1. Extraordinary PhD Award 2014-2015 sponsored by Universitat Politècnica de València.
2. Outstanding Student Paper Awards at International Symposium on Intelligent Signal Processing and Communication Systems, Japan (ISPACS 2013)
3. First National Award for the University Academic Performance Excellence, 2007-2008, sponsored by the Spanish Government.
4. Generalitat Valenciana's Award to the University Academic Performance, 2008.
5. Telecommunications Liberalization Award 2008, in the National Bachelor's Degree Projects Contest, sponsored by the National Association of Telecommunication Engineers, 2008.
6. Special Technical Engineering in Telecommunications Award INTELCO'08, sponsored by the Regional Association of Telecommunication Engineers, 2008.
7. Best Academic Performance Award 2007-2008 sponsored by Universitat Politècnica de València, 2008.
8. Bachelor's Degree Project Award 2008 to the best Digital Television application sponsored by Tecatel.
9. Awarded by the Consejo Social, Universitat Politècnica de València, 2008 for the best academic career in the Escuela Politécnica Superior de Gandia.

C.6. Visiting researcher

- **University/Department:** Electrical and Computer Engineering, University of California, Davis, USA.
  Host: Shu Lin
  Topic: Design of low-complexity soft and hard-decision decoders for very high-rate codes, based on LDPC, Reed-Solomon and Turbo codes. Design and implementation of LDPC decoders for satellite communication systems.
  Duration: April 2013 – July 2013

- **University/Department:** Ecole Nationale Supérieure de l'Electronique et de ses Applications, Cergy-Pontoise, France.
  Host: David Declercq
  Topic: Optimization of a NB-LDPC decoding algorithm based on trellis to obtain high-speed implementations. Design of a symbol flipping algorithm to increase the coding gain in the waterfall region with low complexity**.**
  Duration: Sept. 2012 – Dec. 2012

- **University/Department:** Institut Polytechnique de Bordeaux, Bordeaux, France.
  Host: Camille Leroux
  Topic: Design of a non-binary decoding algorithm for Polar codes.
  Duration: March 2012